

1  
2  
3 SECTION IV  
4 INTERRUPT HANDLING AND WRITE DEFERRAL  
5

6 The 60Hz (50Hz for European version) non-maskable interrupt (NMI)  
7 in the ColecoVision system has a wide variety of applications  
8 such as providing a fixed time base for the timing software, and  
9 a natural debounce interval for the controller interface.  
10 However, interrupts can cause problems if not handled properly.

11 Let us say, for example, that the system is in the midst of a  
12 call to PUTOBJ and is, in fact, writing to VRAM when the  
13 interrupt occurs. If the interrupt service routine calls for  
14 transferring data to another area of VRAM by setting up the VDP  
15 address register (auto-increment) to a different value, the  
16 pending VRAM operation cannot resume properly after the interrupt  
17 is serviced.

18  
19 The OS contains software which allows graphics operations on the  
20 object level to be protected against damage by asynchronous  
21 interrupts. It should be stressed that the OS protects ONLY the  
22  
23  
24  
25  
26

1 object level. Routines on the table and chip driver levels could  
2 be deferred against interrupt by using the application library  
3 routine, DEF\_INT, suggested in ColecoVision Bulletin No. 0010  
4 (Appendix D).

5  
6 In order to implement this protection for graphics operations,  
7 the application program must allocate space for a deferral queue.  
8 The size of this queue depends on the number of graphics  
9 operations that are expected to be performed between NMIs, but  
10 usually fifteen entries of three bytes each will prove  
11 sufficient. The address of the queue should be passed on to the  
12 OS using a routine called INIT\_WRITER which also empties the  
13 queue and prepares it for operation. Thereafter, whenever the  
14 flag byte DEFER\_WRITES is set to true (1), calls to PUTOBJ are  
15 deferred by placing them on the queue where they may be performed  
16 using a single OS call from the interrupt service routine.

17  
18 In addition to the buffer in which the queue resides, the  
19 deferral routines use several defined storage areas in the course  
20 of their operation. These are: QUEUE\_SIZE, QUEUE\_HEAD,  
21 QUEUE\_TAIL, HEAD\_ADDRESS, TAIL\_ADDRESS and BUFFER. They are all  
22 related to the state of the queue.  
23  
24  
25  
26

1  
2  
3  
4  
5  
6  
7  
8  
9  
10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24  
25  
26

4.1 INIT\_WRITER

Calling Sequence:

```
LD    A, SIZE
LD    HL, LOCATION
CALL  INIT_WRITER
```

Description:

INIT\_WRITER initializes the queue. It does not, in fact, do anything to the "physical" queue in RAM. Instead, it merely sets up its description by setting QUEUE\_SIZE to SIZE, HEAD\_ADDRESS and TAIL\_ADDRESS to the beginning of the buffer and QUEUE\_HEAD and QUEUE\_TAIL to 0.

Parameters:

SIZE                    The size in entries of the queue.  
SIZE should be equal to the amount

1 of space allocated for the queue  
2 divided by three. Range for SIZE  
3 is 1 to 255.  
4  
5 LOCATION The location of CRAM area  
6 allocated for the queue.  
7  
8 Side Effects:  
9  
10 - Destroys AF.  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24  
25  
26

1  
2  
3  
4  
5  
6  
7  
8  
9  
10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24  
25  
26

4.2 WRITER

Calling Sequence:

CALL WRITER

Description:

WRITER performs any deferred PUTOBJ operations that may be on the queue emptying the queue as it goes. WRITER should be called by the interrupt service routine.

WRITER uses a "back door" into the PUTOBJ software without ever making an explicit call to PUTOBJ.

Side Effects:

Destroys AF, BC, DE, HL, IX, IY, BC', DE' and HL'.

