```
   1  File:  AN1810.PLD
   2
   3  This file contains the logic necessary for an EP1810 PLD to perform
   4  address decoding and 8/16 bit data I/O interface an IDE hard disk
   5  drive to the Coleco Adam computer as part of an ADAMnet controller.
   6
   7  Inputs:
   8
   9    A0-A3, A10, A11, A12, A14, A15 = 6803 address lines
  10    D0-7   = 6803 data lines (bidirectional)
  11    DD0-7  = Disk Interface data lines (bidirectional)
  12    DD8-15 = Disk Interface data lines (bidirectional)
  13             Inputs to PLD are global via "pin feedback"
  14             Outputs to drive are latched on write to upper byte port
  15    DDL8-15= Disk drive upper byte latched to send on D0-7
  16    ARSI   = ADAMnet reset to go to the 6803 (to be ORed with PORI)
  17    PORI   = Power-On reset to go to the 6803 (to be ORed with ARSI)
  18    E      = 6803 Output Clock
  19    CLKU   = Clock to latch upper data byte to/from drive
  20    ADAI   = ADAMnet serial data to 6803 (after decombining)
  21
  22  Outputs:
  23
  24    CS0    = Lower data byte enable (6803 <-> drive)
  25    CS1    = Lower 8 IO addresses selected on IDE I/F
  26    CS3    = Upper 8 IO addresses selected on IDE I/F
  27    IOR    = Processor wants to read data from one of the IDE ports
  28    IOW    = Processor wants to write data to one of the IDE ports
  29    DRST   = Processor reset to IDE drive
  30    PCE    = PROM Chip Enable
  31    RWE    = RAM Write Enable
  32    RCE    = RAM Chip Enable
  33    ROE    = RAM (& PROM) Output Enable
  34    CLKU   = Clock to latch upper data byte to/from drive
  35    ADIO   = 6803 data to/from ADAMnet (bidirectional)
  36    ADAO   = 6803 data to ADAMnet (before combining)
  37    ARSO   = ADAMnet reset to 6803 processor (PORI ORed with ARSI)
  38
  39  Address Map:
  40
  41    RAM   @ 0400H-07FFH (Write) and 1400H-17FFH (Read)
  42    PROM  @ C000H-FFFFH (Read only)
  43    IDE   @ 0801H-0808H and 080AH-080FH (Read) and
  44            1801H-1808H and 180AH-180FH (Write)
  45
  46    Note:    Because of incomplete address decoding, these devices
  47             also appear at other addresses within the map.
  48
  49
  50                    IDE Register Addreses
  51            _____
  52
  53    Read:                              Write:
  54
  55    0800H = Not decoded                1800H = Drive RESET
  56    0801H = Error Register    1801H = Write Precomp
  57    0802H = Sector count               1802H = Sector count
  58    0803H = Sector number              1803H = Sector number
  59    0804H = Cylinder low byte          1804H = Cylinder low byte
  60    0805H = Cylinder high byte         1805H = Cylinder high byte
  61    0806H = Drive/head                 1806H = Drive/head
  62    0807H = Status Register         1807H = Command Register
  63    0808H = Data Register Low          1808H = Data Register Low
  64    0809H = Data Register High         1809H = Data Register High
  65    080AH = Not Used               180AH = Digital Output (FL)
  66    080BH = Not Used               180BH = Not Used
  67    080CH = Main Status (FL)       180CH = Main Status (FL)
  68    080DH = Diskette data (FL)        180DH = Diskette data (FL)
  69    080EH = Not Used               180EH = Fixed Disk
  70    080FH = Digital Input             180FH = Diskette control
```

```
71
72   Address decoding:
73
74      Because the upper addresses are not completely decoded for each
75      signal produced, the address ranges indicated are actually much
76      larger than indicated (the signal will be produced at additional
77      addresses within the map).  For example, CLKU uses only 3 of the
78      upper eight address lines to decode its range.  The comment says
79      that CLKU is produced at 08X8H, 28X8H, 48X8H, and 68X8H for read
80      access and at 18X9H, 38X9H, 58X9H, and 78X9H for write.  However,
81      the response range for 08X8H is really 08 through 0F on the upper
82      address lines.  Likewise for the other occurances.
83
84      Also, all of the lowest eight address lines are not used either.
85      This means that the signal in question will occur at every
86      16 byte multiple of the address decoded.  Therefore, using the
87      CLKU example of above, the signal will be produced at 0808H,
88      0818H, 0828H, 0838H, 0848H, 0858H and so on through 08F8H (and
89      because of the upper byte decoding, also at 0908H through 09F8H,
90      and at 0AX8H, 0BX8H, 0CX8H, 0DX8H, 0EX8H, and 0FX8H).
91
92      This is the way that Coleco decoded its memory, so it should not
93      be a problem, as long as the code does not read or write a memory
94      address that produces an unwanted signal occurance.
95
96   For 6803 to send 16 bit data:
97      First send upper byte to address 1809H and latch it into D8-D15
98         flip-flops with CLKU, but do not enable D0-7 drive/processor
99         interface or D8-D15 FF outputs (also, do not send IOW)
100     Then send lower byte to address 1808H, enable D0-7 processor
101        interface and D8-D15 flip-flop outputs (send IOW)
102
103  For 6803 to receive 16 bit data:
104     First read lower byte from address 1808H by sending IOR and
105        enabling D0-7 drive/processor outputs (latch the upper byte
106        into D0-D7 flip-flops with CLKU)
107     Then read the upper byte from address 1809H by enabling D0-D7
108        flip-flops; do not enable D0-7 drive/processor interface and
109        do not send IOR
110
111  |EP1810c
112  |  2:DD0,  3:DD1,  4:DD2,  5:DD3,  6:DDL8,  7:DDL9,  8:DDL10,  9:DDL11,
113  |  10:D0,  11:D1,     12:D2,  13:D3,  14:E,  15:DDEN,  16:PORI,  17:CLK1,
114  |  19:CLK2,  20:A1,  21:A2,  22:A3,  23:D4,  24:D5,  25:D6,  26:D7,  27:DD4,
115  |  28:DD5,  29:DD6,  30:DD7,  31:DDL12,  32:DDL13,  33:DDL14,  34:DDL15,
116  |  36:CS0,  37:CS1,  38:CS3,  39:DRST,  40:IOR,  41:IOW,  42:CLKU,
117  |  43:PCE,  44:DD8,  45:DD9,  46:DD10,  47:DD11,  48:A0,  49:A10,
118  |  50:A11,  51:CLK3,  53:CLK4,  54:A12,  55:A14,  56:A15,  57:DD12,

119  |  58:DD13,  59:DD14,  60:DD15,  61:RCE,  62:RWE,  63:ROE,  64:ARSI,
120  |  65:ADIO,  66:ADAO,  67:ARSO,  68:ADAI
121
122  |  Low:    IOW, IOR, CS0, CS1, CS3, DRST, CLKU, RCE, RWE, ROE, PCE,
123  |          ARSO, ARSI, ADAI, ADAO
124
125  |  Configuration:   "Pin feedback", D[0..7], DD[0..15], ADIO
126  |  Configuration:   "Turbo:1"
127
128  CLKU:
129     upper 8 data bit latch clock; responds to addresses:
130     08X8H, 28X8H, 48X8H, and 68X8H (read lower byte) and
131     18X9H, 38X9H, 58X9H, and 78X9H (write upper byte)
132  |  CLKU
133  |    = (A15' & A12' & A11 & A[3..0]==8H)          |0, 2, 4, 6
134  |    # (A15' & A12 & A11 & A[3..0]==9H)           |1, 3, 5, 7
135
136  CS1:
137     IDE lower 8 registers;   responds to address ranges:
138     08X1H-08X8H, 28X1H-28X8H, 48X1H-48X8H, 68X1H-68X8H, and
139     18X1H-18X8H, 38X1H-38X8H, 58X1H-58X8H, 78X1H-78X8H
140  |  CS1
141  |    = (A15' & A12' & A11 & A[3..0]>=1H & A[3..0]<=8H)   |0, 2, 4, 6
142  |    # (A15' & A12 & A11 & A[3..0]>=1H & A[3..0]<=8H)    |1, 3, 5, 7
```

```
143
144   CS3:
145     IDE upper 8 registers;   responds to address ranges:
146     08XAH-08XFH, 28XAH-28XFH, 48XAH-48XFH, 68XAH-68XFH, and
147     18XAH-18XFH, 38XAH-38XFH, 58XAH-58XFH, 78XAH-78XFH
148   | CS3
149   |   = (A15' & A12' & A11 & A[3..0]>=0AH & A[3..0]<=0FH)  |0, 2, 4, 6
150   |   # (A15' & A12 & A11 & A[3..0]>=0AH & A[3..0]<=0FH)   |1, 3, 5, 7
151
152   DRST:
153     Drive RESET; issued for write to address 18X0H
154   | DRST  = A15' & A12 & A11 & A[3..0]==0H                 |1, 3, 5, 7
155
156   IOW:
157     IO Write signal to drive; issued for addresses 18X1H-18X8H
158     and 18XAH-18XFH (also decoded at MSB = 03, 05, and 07)
159   | IOW
160   |   = (A15' & A12 & A11 & A[3..0]>=1H & A[3..0]<=8H)     |01H-08H
161   |   # (A15' & A12 & A11 & A[3..0]>=0AH & A[3..0]<=0FH)   |0AH-0FH
162
163   IOR:
164     IO Read signal to drive; issued for addresses 08X1H-08X8H
165     and 08XAH-08XFH (also decoded at MSB = 02, 04, and 06)
166   | IOR
167   |   = (A15' & A12' & A11 & A[3..0]>=1H & A[3..0]<=8H)    |01H-08H
168   |   # (A15' & A12' & A11 & A[3..0]>=0AH & A[3..0]<=0FH)  |0AH-0FH
169
170   PCE:
171     PROM Chip Enable; address range C000H-FFFFH
172   | PCE   = A14 & A15
173
174   RWE:
175     RAM Write Enable; address range 0400H-07FFH (Also responds
176     to 2400-27FF, 4400-47FF, 6400-67FF, 8400-87FF, & A400-A7FF)
177   | RWE   = (E & A14' & A10 & A12') # (E & A15' & A10 & A12')
178


179   RCE:
180     RAM Chip Enable; address ranges 0400H-07FFH & 1400H-17FFH
181     (responds to 2nd and 4th quadrants in all upper byte ranges
182     from 00 through 0B)
183   | RCE   = (A14' & A10) # (A15' & A10)
184
185   ROE:
186     RAM Output Enable (on every positive half of clock cycle)
187   | ROE   = E
188
189   D0-7:
190     Processor data bits 0-7 or latched drive data bits 8-15
191     D0-7 outputs are enabled (via the conditioning statement)
192     whenever have an access to 0800H-0FFFH, 2800H-2FFFH,
193     4800H-4FFFH, or 6800H-6FFFH (Read IDE registers).  The
194     data to be output depends on the address selected.
195   | Conditioning: (A15' & A12' & A11) ?? D[0..7]
196   | D0 = (DD0 & A15' & A12' & A11 & A[3..0]==8H)
197   |    # (DDL8 & A15' & A12' & A11 & A[3..0]==9H)
198   | D1 = (DD1 & A15' & A12' & A11 & A[3..0]==8H)
199   |    # (DDL9 & A15' & A12' & A11 & A[3..0]==9H)
200   | D2 = (DD2 & A15' & A12' & A11 & A[3..0]==8H)
201   |    # (DDL10 & A15' & A12' & A11 & A[3..0]==9H)
202   | D3 = (DD3 & A15' & A12' & A11 & A[3..0]==8H)
203   |    # (DDL11 & A15' & A12' & A11 & A[3..0]==9H)
204   | D4 = (DD4 & A15' & A12' & A11 & A[3..0]==8H)
205   |    # (DDL12 & A15' & A12' & A11 & A[3..0]==9H)
206   | D5 = (DD5 & A15' & A12' & A11 & A[3..0]==8H)
207   |    # (DDL13 & A15' & A12' & A11 & A[3..0]==9H)
208   | D6 = (DD6 & A15' & A12' & A11 & A[3..0]==8H)
209   |    # (DDL14 & A15' & A12' & A11 & A[3..0]==9H)
210   | D7 = (DD7 & A15' & A12' & A11 & A[3..0]==8H)
211   |    # (DDL15 & A15' & A12' & A11 & A[3..0]==9H)
212
213   DD0-7:
214     Drive data bits 0-7; DD0-7 outputs are enabled (via the
```

```
215    conditioning statement and signal CS0) whenever we want
216    to write to the IDE registers by accessing 1800H-1FFFH,
217    3800H-3FFFH, 5800H-5FFFH, or 7800H-7FFFH (except register
218    XX09H, the upper byte data register).
219  CS0:
220    DD0-DD7 output enable; responds to address ranges:
221    1801H-1808H and 180AH-180FH (also upper byte = 03, 05,
222    and 07H).
223  | CS0  = (A15' & A12 & A11 & A[3..0]>=1H & A[3..0]<=8H)
224  |       # (A15' & A12 & A11 & A[3..0]>=0AH & A[3..0]<=0FH)
225  | Conditioning: DDEN ?? DD[0..7]        |DDEN connected to CS0 on PCB
226  | DD[0..7] = D[0..7]
227
228  | DDL[8..11]  = dff(DD[8..11],CLK1)   |D8-11 -> D0-3 FFs on CLKU
229  | DDL[12..15] = dff(DD[12..15],CLK2)  |D12-15 -> D4-7 FFs on CLKU
230
231  DD8-15:
232    Drive data bits 8-15; outputs are enabled (via the
233    conditioning statement) when we output a data byte to
234    the lower byte (address 1808H).  We assume that the
235    upper byte had been latched previously (by a write to
236    address 0809H).
237  | Conditioning: (A15' & A12 & A11 & A[3..0]==8H) ?? DD[8..15]
238  | DD[8..11]   = dff(D[0..3],CLK3)     |D0-3 -> DD8-11 FFs on CLKU

239  | DD[12..15]  = dff(D[4..7],CLK4)     |D4-7 -> DD12-15 FFs on CLKU
240
241  ADIO:
242    ADAMnet IO line; ADAO from the processor drives the net;
243    ADAI is the input to the processor from the net.
244  | Conditioning: ADAO' ?? ADIO   |ADAO enables output: +5V or open
245  | ADIO  = ADAO'                  |ADIO=TS for ADAO=H, ADIO=H for ADAO=L
246  | ADAI  = ADIO                   |fed from ADAMnet IO line; input to 6803
247
248  ARSO:
249    Processor RESET; driven by OR of ADAMnet RESET (ARSI) and
250    Power ON RESET (PORI)
251  | ARSO  = PORI # ARSI
252
253  | Signature: "ANETide0"
```

RESOLVED EXPRESSIONS (Reduction 2)

Signal name	Row	Terms
CLKU	300	A1' A2' A3 A0' A11 A12' A15'
	301	A1' A2' A3 A0 A11 A12 A15'
CS1	250	A1' A2' A3 A0' A11 A15'
	251	A1 A3' A11 A15'
	252	A2 A3' A11 A15'
	253	A3' A0 A11 A15'
CS3	260	A1 A3 A11 A15'
	261	A2 A3 A11 A15'
DRST	270	A1' A2' A3' A0' A11 A12 A15'
IOW	290	A3' A0 A11 A12 A15'
	291	A3 A0' A11 A12 A15'
	292	A1 A11 A12 A15'
	293	A2 A11 A12 A15'
IOR	280	A3' A0 A11 A12' A15'
	281	A3 A0' A11 A12' A15'
	282	A1 A11 A12' A15'
	283	A2 A11 A12' A15'
PCE	310	A14 A15
RWE	410	E A10 A12' A14'

```
                411   E   A10   A12'  A15'

RCE             400   A10   A14'
                401   A10   A15'

ROE             420   E

D0               89   A11   A12'  A15'
                 80   DD0   A1'  A2'  A3   A0'  A11   A12'  A15'
                 81   DDL8  A1'  A2'  A3   A0   A11   A12'  A15'

D1               99   A11   A12'  A15'
                 90   DD1   A1'  A2'  A3   A0'  A11   A12'  A15'
                 91   DDL9  A1'  A2'  A3   A0   A11   A12'  A15'

D2              109   A11   A12'  A15'
                100   DD2   A1'  A2'  A3   A0'  A11   A12'  A15'
                101   DDL10 A1'  A2'  A3   A0   A11   A12'  A15'

D3              119   A11   A12'  A15'
                110   DD3   A1'  A2'  A3   A0'  A11   A12'  A15'
                111   DDL11 A1'  A2'  A3   A0   A11   A12'  A15'

D4              129   A11   A12'  A15'
                120   A1'  A2'  A3   DD4   A0'  A11   A12'  A15'
                121   A1'  A2'  A3   DDL12 A0   A11   A12'  A15'

D5              139   A11   A12'  A15'
                130   A1'  A2'  A3   DD5   A0'  A11   A12'  A15'
                131   A1'  A2'  A3   DDL13 A0   A11   A12'  A15'
D6              149   A11   A12'  A15'
                140   A1'  A2'  A3   DD6   A0'  A11   A12'  A15'
                141   A1'  A2'  A3   DDL14 A0   A11   A12'  A15'

D7              159   A11   A12'  A15'
                150   A1'  A2'  A3   DD7   A0'  A11   A12'  A15'
                151   A1'  A2'  A3   DDL15 A0   A11   A12'  A15'

CS0             240   A3'  A0   A11   A12   A15'
                241   A3   A0'  A11   A12   A15'
                242   A1   A11   A12   A15'
                243   A2   A11   A12   A15'

DD0               9   DDEN
                  0   D0

DD1              19   DDEN
                 10   D1

DD2              29   DDEN
                 20   D2

DD3              39   DDEN
                 30   D3

DD4             169   DDEN
                160   D4

DD5             179   DDEN
                170   D5

DD6             189   DDEN
                180   D6

DD7             199   DDEN
                190   D7

DDL8             40   DD8

DDL9             50   DD9

DDL10            60   DD10
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DDL11              70    DD11

DDL12             200    DD12

DDL13             210    DD13

DDL14             220    DD14

DDL15             230    DD15

DD8               329    A1'  A2'  A3   A0'  A11   A12   A15'
                  320    D0

DD9               339    A1'  A2'  A3   A0'  A11   A12   A15'
                  330    D1


♀DD10             349    A1'  A2'  A3   A0'  A11   A12   A15'
                  340    D2

DD11              359    A1'  A2'  A3   A0'  A11   A12   A15'
                  350    D3

DD12              369    A1'  A2'  A3   A0'  A11   A12   A15'
                  360    D4

DD13              379    A1'  A2'  A3   A0'  A11   A12   A15'
                  370    D5

DD14              389    A1'  A2'  A3   A0'  A11   A12   A15'
                  380    D6

DD15              399    A1'  A2'  A3   A0'  A11   A12   A15'
                  390    D7

ADI0              449    ADA0'
                  440    ADA0'

ADAI              470    ADI0

ARS0              460    PORI
                  461    ARSI
```

SIGNAL ASSIGNMENT

Pin	Signal name	Column	Beg	Avail	Used	Activity	
				Rows			
2.	DD0	23	0	10	2	High	(Three-state)
3.	DD1	21	10	10	2	High	(Three-state)
4.	DD2	19	20	10	2	High	(Three-state)
5.	DD3	17	30	10	2	High	(Three-state)
6.	DDL8	15	40	10	1	High	(Registered)
7.	DDL9	13	50	10	1	High	(Registered)
8.	DDL10	11	60	10	1	High	(Registered)
9.	DDL11	9	70	10	1	High	(Registered)
10.	D0	47	80	10	3	High	(Three-state)
11.	D1	45	90	10	3	High	(Three-state)
12.	D2	43	100	10	3	High	(Three-state)
13.	D3	41	110	10	3	High	(Three-state)
14.	E	73	-	-	-	High	
15.	DDEN	71	-	-	-	High	
16.	PORI	69	-	-	-	High	
17.	CLK1	85	-	-	-	High	(Clock)
19.	CLK2	83	-	-	-	High	(Clock)
20.	A1	63	-	-	-	High	
21.	A2	65	-	-	-	High	
22.	A3	67	-	-	-	High	
23.	D4	33	120	10	3	High	(Three-state)
24.	D5	35	130	10	3	High	(Three-state)

25.	D6	37	140	10	3	High	(Three-state)
26.	D7	39	150	10	3	High	(Three-state)
27.	DD4	9	160	10	2	High	(Three-state)
28.	DD5	11	170	10	2	High	(Three-state)
29.	DD6	13	180	10	2	High	(Three-state)
30.	DD7	15	190	10	2	High	(Three-state)
31.	DDL12	17	200	10	1	High	(Registered)
32.	DDL13	19	210	10	1	High	(Registered)
33.	DDL14	21	220	10	1	High	(Registered)
34.	DDL15	23	230	10	1	High	(Registered)
36.	CS0	22	240	10	4	Low	(Three-state)
37.	CS1	20	250	10	4	Low	(Three-state)
38.	CS3	18	260	10	2	Low	(Three-state)
39.	DRST	16	270	10	1	Low	(Three-state)
40.	IOR	14	280	10	4	Low	(Three-state)
41.	IOW	12	290	10	4	Low	(Three-state)
42.	CLKU	10	300	10	2	Low	(Three-state)
43.	PCE	8	310	10	1	Low	(Three-state)
44.	DD8	31	320	10	2	High	(Registered)
45.	DD9	29	330	10	2	High	(Registered)
46.	DD10	27	340	10	2	High	(Registered)
47.	DD11	25	350	10	2	High	(Registered)
48.	A0	61	–	–	–	High	
49.	A10	59	–	–	–	High	
50.	A11	57	–	–	–	High	
51.	CLK3	81	–	–	–	High	(Clock)
53.	CLK4	87	–	–	–	High	(Clock)
54.	A12	75	–	–	–	High	
55.	A14	77	–	–	–	High	
56.	A15	79	–	–	–	High	
57.	DD12	49	360	10	2	High	(Registered)
58.	DD13	51	370	10	2	High	(Registered)
59.	DD14	53	380	10	2	High	(Registered)
60.	DD15	55	390	10	2	High	(Registered)
61.	RCE	8	400	10	2	Low	(Three-state)
62.	RWE	10	410	10	2	Low	(Three-state)
63.	ROE	12	420	10	1	Low	(Three-state)
64.	ARSI	14	430	10	0	Low	(Three-state)
65.	ADIO	17	440	10	2	High	(Three-state)
66.	ADAO	18	450	10	0	Low	(Three-state)
67.	ARSO	20	460	10	2	Low	(Three-state)
68.	ADAI	22	470	10	1	Low	(Three-state)
69.	–	7	80	10	0		(Three-state)
70.	–	5	90	10	0		(Three-state)
71.	–	3	100	10	0		(Three-state)
72.	–	1	110	10	0		(Three-state)
73.	–	1	120	10	0		(Three-state)
74.	–	3	130	10	0		(Three-state)
75.	–	5	140	10	0		(Three-state)
76.	–	7	150	10	0		(Three-state)
77.	–	7	320	10	0		(Three-state)
78.	–	5	330	10	0		(Three-state)
79.	–	3	340	10	0		(Three-state)
80.	–	1	350	10	0		(Three-state)
81.	–	1	360	10	0		(Three-state)
82.	–	3	370	10	0		(Three-state)
83.	–	5	380	10	0		(Three-state)
84.	–	7	390	10	0		(Three-state)

```
                                    ---- ----
                                    640   96  (15%)
```

I200 No fatal errors found in source code.
I201 No warnings.

```
♀OrCAD PLD-386
Type:      EP1810c
*
QP68* QF42490* QV1024*
F0*
```

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L01672 1111111111111111111111111111111111111111111111111111111111111111110111111111111111111111*
L01760 1111111111111111111111111111111111111110111111111111111111111111111111111111111111111111*
L02552 1111111111111111111111111111111111111111111111111111111111111111111011111111111111111111*
L02640 1111111111111111111111111111111111111111101111111111111111111111111111111111111111111111*
L03432 1111111111111111111111111111111111111111111111111111111111111111101111111111111111111111*
L03520 1111111111111111111111111111110111111111111111111111111111111111111111111111111111111111*
L04312 1111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L04400 1111111111111111111111111111101111111111111111111111111111111111111111111111111111111111*
L05192 1111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L05280 1111111111111111111111111111101111111111111111111111111111111111111111111111111111111111*
L06072 1111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
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L42328 0010000100001001110011100111001100000000000000000000000000000000000001000110001100011*
L42416 0001100011000110001100010000000000001000010000100000000000000000000011*
CE183*
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I202 7/5/92 12:39 pm (Sunday)
I203 Memory usage 98K
I204 Elapsed time 9 seconds