```
OrCAD PLD COMPILER  V4.02   2/7/91  (Source file .\FDRV0G1.PLD)

  1  This file contains the logic necessary for a GAL16V8 to perform I/O
  2  Decoding for the Micro Innovations Adamnet Floppy Disk Drive.
  3
  4
  5  I/O Pin Definitions:
  6
  7  |GAL16V8   1:A9,           2:A10,          3:A11,          4:A12,
  8  |          5:A13,          6:A14,          7:A15,          8:RW,
  9  |          9:E,            11:EPrime,      12:FDCRE,       13:FDCWE,
 10  |          14:FDCA0,       15:FDCA1,       16:OECLK,       17:PROMCE,
 11  |          18:RAMWE,       19:RAMCE
 12
 13  Acronyms:
 14
 15     Inputs -
 16
 17     A9-A15  = 6803 Address Lines A9 - A15
 18     RW      = 6803 Read/Write Line
 19     E       = 6803 Output Clock (2Mhz)
 20     EPrime  = Delayed 6803 Output Clock
 21
 22     Outputs:
 23
 24     FDCRE   = Read Enable line to 2793 FDC
 25     FDCWE   = Write Enable line to 2793 FDC
 26     FDCA0   = Address 0 line to 2793 FDC
 27     FDCRE   = Address 1 line to 2793 FDC
 28     OECLK   = RAM/PROM Output Enable & FDC Clock
 29     PROMCE  = PROM Chip Enable
 30     RAMWE   = RAM Write Enable
 31     RAMCE   = RAM Chip Enable
 32
 33  |  High: A[9..15], RW, E, EPrime
 34  |
 35  |  FDCRE   = (E & A14' & A11 & A12') # (E & A15' & A11 & A12')
 36  |  FDCWE   = (E & A14' & A11 & A12) # (E & A15' & A11 & A12)
 37  |  FDCA0   = A13'
 38  |  FDCA1   = A14'
 39  |  OECLK   = E
 40  |  PROMCE  = A14 & A15
 41  |  RAMWE   = (E & A14' & A10 & A12') # (E & A15' & A10 & A12')
 42  |  RAMCE   = (A14' & A10) # (A15' & A10)
 43  |
 44  |  Signature: "FDRVrev1"
I289  Complex GAL architecture selected.


♀RESOLVED EXPRESSIONS (Reduction 2)

Signal name      Row   Terms

FDCRE             57   A11  A12' A14' E
                  58   A11  A12' A15' E

FDCWE             49   A11  A12  A14' E
                  50   A11  A12  A15' E

FDCA0             41   A13'

FDCA1             33   A14'
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```
OECLK              25   E

PROMCE             17   A14  A15

RAMWE               9   A10  A12' A14' E
                   10   A10  A12' A15' E

RAMCE               1   A10  A14'
                    2   A10  A15'
```

♀SIGNAL ASSIGNMENT

Pin	Signal name	Column	Rows Beg	Rows Avail	Rows Used	Activity	
1.	A9	2	-	-	-	High	(Clock)
2.	A10	0	-	-	-	High	
3.	A11	4	-	-	-	High	
4.	A12	8	-	-	-	High	
5.	A13	12	-	-	-	High	
6.	A14	16	-	-	-	High	
7.	A15	20	-	-	-	High	
8.	RW	24	-	-	-	High	
9.	E	28	-	-	-	High	
11.	EPrime	30	-	-	-	High	(Enable)
12.	FDCRE	1	56	8	2	Low	(Three-state)
13.	FDCWE	27	48	8	2	Low	(Three-state)
14.	FDCA0	23	40	8	1	Low	(Three-state)
15.	FDCA1	19	32	8	1	Low	(Three-state)
16.	OECLK	15	24	8	1	Low	(Three-state)
17.	PROMCE	11	16	8	1	Low	(Three-state)
18.	RAMWE	7	8	8	2	Low	(Three-state)
19.	RAMCE	1	0	8	2	Low	(Three-state)
				64	12	(19%)	

```
W320  Signal RW is not used in the final equations.

I200  No fatal errors found in source code.
I201  One warning.
```

♀OrCAD PLD

```
Type:       GAL16V8
*
QP20* QF2194* QV1024*
F0*
L0000 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0032 01 11 11 11 11 11 11 11 10 11 11 11 11 11 11 11 *
L0064 01 11 11 11 11 11 11 11 11 11 10 11 11 11 11 11 *
L0256 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0288 01 11 11 11 10 11 11 11 10 11 11 11 11 11 01 11 *
L0320 01 11 11 11 10 11 11 11 11 11 10 11 11 11 01 11 *
L0512 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0544 11 11 11 11 11 11 11 11 01 11 01 11 11 11 11 11 *
L0768 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0800 11 11 11 11 11 11 11 11 11 11 11 11 11 11 01 11 *
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L1024 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L1056 11 11 11 11 11 11 11 11 10 11 11 11 11 11 11 11 *
L1280 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L1312 11 11 11 11 11 11 10 11 11 11 11 11 11 11 11 11 *
L1536 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L1568 11 11 01 11 01 11 11 11 10 11 11 11 11 11 01 11 *
L1600 11 11 01 11 01 11 11 11 11 11 10 11 11 11 01 11 *
L1792 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L1824 11 11 01 11 10 11 11 11 10 11 11 11 11 11 01 11 *
L1856 11 11 01 11 10 11 11 11 11 11 10 11 11 11 01 11 *
L2048 00 00 00 00 01 00 01 10 01 00 01 00 01 01 00 10 *
L2080 01 01 01 10 01 11 00 10 01 10 01 01 01 11 01 10 *
L2112 00 11 00 01 11 11 11 11 11 11 11 11 11 11 11 11 *
L2144 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L2176 11 11 11 11 11 11 11 11 11 *
C5A57*

I202  12/26/91  2:41 pm  (Thursday)
I203  Memory utilization 2198/22374 (10%)
I204  Elapsed time 3 seconds
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