```
OrCAD PLD COMPILER-386 V1.00  11/25/91  (Source file .\HF4DD_G1.PLD)

  1  File:      HF4DD_G1
  2  Date:      June 21, 1992
  3
  4  This file contains the logic necessary for a GAL16V8 to perform I/O
  5  Decoding for the Micro Innovations High Density controller board
  6  (PN: FC115E), with a 4 Mhz clock, installed in a 320K or 720K Adamnet
  7  Floppy Disk Drive.
  8
  9
 10  I/O Pin Definitions:
 11
 12  |GAL16V8   2:E,            3:A10,          4:A11,          5:A12,
 13  |          6:A14,          7:A15,          9:EPrime,       14:PROMCE,
 14  |          16:RAMWE,       17:RAMCE,       18:FDCWE,       19:FDCRE
 15
 16  Acronyms:
 17
 18     Inputs -
 19
 20     A10-A15 = 6803 Address Lines A10 - A15 (A13 not used)
 21     E       = 6803 Output Clock (2Mhz)
 22     EPrime  = Delayed 6803 Output Clock (250 ns late)
 23
 24     Outputs:
 25
 26     FDCRE   = Read Enable line to 2793 FDC
 27     FDCWE   = Write Enable line to 2793 FDC
 28     PROMCE  = PROM Chip Enable
 29     RAMWE   = RAM Write Enable
 30     RAMCE   = RAM Chip Enable
 31
 32  |  High:   A10, A11, A12, A14, A15, E, EPrime
 33  |
 34  |  FDCRE   = (E & A14' & A11 & A12') # (E & A15' & A11 & A12')
 35  |  FDCWE   = (EPrime' & A14' & A11 & A12)
 36  |          # (EPrime' & A15' & A11 & A12)
 37  |  PROMCE  = A14 & A15
 38  |  RAMWE   = (E & A14' & A10 & A12') # (E & A15' & A10 & A12')
 39  |  RAMCE   = (A14' & A10) # (A15' & A10)
 40  |
 41  |  Signature: "HF4DD r1"
I289  Complex GAL architecture selected.


♀RESOLVED EXPRESSIONS (Reduction 2)

Signal name      Row   Terms

FDCRE             1   E  A11  A12' A14'
                  2   E  A11  A12' A15'

FDCWE             9   A11  A12  A14' EPrime'
                 10   A11  A12  A15' EPrime'

PROMCE           41   A14  A15

RAMWE            25   E  A10  A12' A14'
                 26   E  A10  A12' A15'

RAMCE            17   A10  A14'
```

18 A10 A15'

SIGNAL ASSIGNMENT

Pin	Signal name	Column	Rows Beg	Rows Avail	Rows Used	Activity	
1.	-	2	-	-	-		(Clock)
2.	E	0	-	-	-	High	
3.	A10	4	-	-	-	High	
4.	A11	8	-	-	-	High	
5.	A12	12	-	-	-	High	
6.	A14	16	-	-	-	High	
7.	A15	20	-	-	-	High	
8.	-	24	-	-	-		
9.	EPrime	28	-	-	-	High	
11.	-	30	-	-	-		(Enable)
12.	-	-	56	8	0		(Three-state)
13.	-	26	48	8	0		(Three-state)
14.	PROMCE	23	40	8	1	Low	(Three-state)
15.	-	18	32	8	0		(Three-state)
16.	RAMWE	15	24	8	2	Low	(Three-state)
17.	RAMCE	11	16	8	2	Low	(Three-state)
18.	FDCWE	7	8	8	2	Low	(Three-state)
19.	FDCRE	1	0	8	2	Low	(Three-state)
				64	9	(14%)	

I200 No fatal errors found in source code.
I201 No warnings.

♀OrCAD PLD-386
Type: GAL16V8
*
QP20* QF2194* QV1024*
F0*
L0000 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0032 01 11 11 11 01 11 10 11 10 11 11 11 11 11 11 11 *
L0064 01 11 11 11 01 11 10 11 11 11 10 11 11 11 11 11 *
L0256 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0288 11 11 11 11 01 11 01 11 10 11 11 11 11 11 10 11 *
L0320 11 11 11 11 01 11 01 11 11 11 10 11 11 11 10 11 *
L0512 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0544 11 11 01 11 11 11 11 11 10 11 11 11 11 11 11 11 *
L0576 11 11 01 11 11 11 11 11 11 11 10 11 11 11 11 11 *
L0768 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0800 01 11 01 11 11 11 10 11 10 11 11 11 11 11 11 11 *
L0832 01 11 01 11 11 11 10 11 11 11 10 11 11 11 11 11 *
L1280 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L1312 11 11 11 11 11 11 11 11 01 11 01 11 11 11 11 11 *
L2048 00 00 10 11 01 00 10 00 01 00 01 10 00 11 01 00 *
L2080 01 00 01 00 01 00 01 00 00 10 00 00 01 11 00 10 *
L2112 00 11 00 01 11 11 11 11 11 11 11 11 11 11 11 11 *
L2144 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L2176 11 11 11 11 11 11 11 11 11 *
C4193*

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I202  6/21/92  3:30 pm  (Sunday)
I203  Memory usage 24K
I204  Elapsed time 1 second

♀
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