OrCAD PLD COMPILER-386 V1.00 11/25/91 (Source file .\HF8HD_G1.PLD)

```
  1  File:      HF8HD_G1
  2  Date:      June 21, 1992
  3
  4  This file contains the logic necessary for a GAL16V8 to perform I/O
  5  Decoding for the Micro Innovations 1.4MB Adamnet Floppy Disk Drive
  6  (controller board FC115E with an 8 Mhz clock and high density drive).
  7
  8  I/O Pin Definitions:
  9
 10  |GAL16V8   1:CLKIN,        2:E,            3:A10,          4:A11,
 11  |          5:A12,          6:A14,          7:A15,          8:RESET,
 12  |          9:Eprime,       11:ENABLE,      12:Q0,          13:Q1,
 13  |          14:PROMCE,      15:ACLK,        16:RAMWE,       17:RAMCE,
 14  |          18:FDCWE,       19:FDCRE
 15  |
 16  |  Registers:  ENABLE ?? CLKIN // Q[1..0]
 17
 18  Acronyms:
 19
 20     Inputs -
 21
 22     A10-A15 = 6803 Address Lines A10 - A15 (A13 not used)
 23     CLKIN   = 2Mhz 6803 Output Clock (used to produce Q0 & Q1)
 24     ENABLE  = Q0 & Q1 output enable line (grounded in layout design)
 25     RESET   = Reset to the 6803
 26     E       = 2Mhz 6803 Output Clock (Same as CLKIN)
 27     Eprime  = Delayed 6803 Output Clock (250 ns late)
 28
 29     Outputs:
 30
 31     FDCRE   = Read Enable line to 2793 FDC
 32     FDCWE   = Write Enable line to 2793 FDC
 33     ACLK    = ADAMnet serial port clock (Q1) gated by RESET
 34               (output = 0 when RESET = 1, clock otherwise)
 35     PROMCE  = PROM Chip Enable
 36     RAMWE   = RAM Write Enable
 37     RAMCE   = RAM Chip Enable
 38     Q0      = 1Mhz clock out (2 Mhz E clock divided by 2)
 39     Q1      = 500Khz clock out (E clock divided by 4)
 40               (used as serial port clock input, to P22)
 41
 42  |  High:   A10, A11, A12, A14, A15, E, EPrime, RESET, Q0, Q1, ACLK,
 43  |          CLKIN
 44  |
 45  |  FDCRE   = (E & A14' & A11 & A12') # (E & A15' & A11 & A12')
 46  |  FDCWE   = (Eprime' & A14' & A11 & A12)
 47  |          # (Eprime' & A15' & A11 & A12)
 48  |  ACLK    = Q1 & RESET'
 49  |  PROMCE  = A14 & A15
 50  |  RAMWE   = (E & A14' & A10 & A12') # (E & A15' & A10 & A12')
 51  |  RAMCE   = (A14' & A10) # (A15' & A10)
 52  |
 53  |  Map:    Q[1..0] -> Q[1..0]  {n -> n+1}
 54  |
 55  |  Signature: "HF8HD r1"

♀I289  Registered GAL architecture selected.


RESOLVED EXPRESSIONS (Reduction 2)
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```
Signal name      Row   Terms

FDCRE             1   E  A11  A12' A14'
                  2   E  A11  A12' A15'

FDCWE             9   A11  A12  A14' Eprime'
                 10   A11  A12  A15' Eprime'

ACLK             33   RESET' Q1

PROMCE           41   A14  A15

RAMWE            25   E  A10  A12' A14'
                 26   E  A10  A12' A15'

RAMCE            17   A10  A14'
                 18   A10  A15'

Q1               48   Q0' Q1
                 49   Q0  Q1'

Q0               56   Q0'
```

♀SIGNAL ASSIGNMENT

Pin	Signal name	Column	Rows Beg	Rows Avail	Rows Used	Activity	
1.	CLKIN	0	-	-	-	High	(Clock)
2.	E	0	-	-	-	High	
3.	A10	4	-	-	-	High	
4.	A11	8	-	-	-	High	
5.	A12	12	-	-	-	High	
6.	A14	16	-	-	-	High	
7.	A15	20	-	-	-	High	
8.	RESET	24	-	-	-	High	
9.	Eprime	28	-	-	-	High	
11.	ENABLE	1	-	-	-	Low	(Enable)
12.	Q0	30	56	8	1	High	(Registered)
13.	Q1	26	48	8	2	High	(Registered)
14.	PROMCE	23	40	8	1	Low	(Three-state)
15.	ACLK	18	32	8	1	High	(Three-state)
16.	RAMWE	15	24	8	2	Low	(Three-state)
17.	RAMCE	11	16	8	2	Low	(Three-state)
18.	FDCWE	7	8	8	2	Low	(Three-state)
19.	FDCRE	3	0	8	2	Low	(Three-state)
				64	13	(20%)	

```
I200  No fatal errors found in source code.
I201  No warnings.
```

```
♀OrCAD PLD-386
Type:       GAL16V8
*
QP20* QF2194* QV1024*
```

```
F0*
L0000 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0032 01 11 11 11 01 11 10 11 10 11 11 11 11 11 11 11 *
L0064 01 11 11 11 01 11 10 11 11 11 10 11 11 11 11 11 *
L0256 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0288 11 11 11 11 01 11 01 11 10 11 11 11 11 11 10 11 *
L0320 11 11 11 11 01 11 01 11 11 11 10 11 11 11 10 11 *
L0512 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0544 11 11 01 11 11 11 11 11 10 11 11 11 11 11 11 11 *
L0576 11 11 01 11 11 11 11 11 11 11 10 11 11 11 11 11 *
L0768 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0800 01 11 01 11 11 11 10 11 10 11 11 11 11 11 11 11 *
L0832 01 11 01 11 11 11 10 11 11 11 10 11 11 11 11 11 *
L1024 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L1056 11 11 11 11 11 11 11 11 11 11 11 11 10 01 11 11 *
L1280 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L1312 11 11 11 11 11 11 11 11 01 11 01 11 11 11 11 11 *
L1536 11 11 11 11 11 11 11 11 11 11 11 11 11 01 11 10 *
L1568 11 11 11 11 11 11 11 11 11 11 11 11 11 10 11 01 *
L1792 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 10 *
L2048 00 00 10 11 01 00 10 00 01 00 01 10 00 11 10 00 *
L2080 01 00 10 00 01 00 01 00 00 10 00 00 01 11 00 10 *
L2112 00 11 00 01 11 11 11 00 11 11 11 11 11 11 11 11 *
L2144 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L2176 11 11 11 11 11 11 11 11 01 *
C534C*

I202  7/21/92  8:05 pm  (Tuesday)
I203  Memory usage 27K
I204  Elapsed time 1 second

♀
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