OrCAD PLD COMPILER V4.02 2/7/91 (Source file .\2MU1V10.PLD)

```
  1  This file contains the logic necessary for a GAL22V10 to latch data bits
  2  D0-D4 and multiplex the lowest three and the uppermost address lines
  3  (MA0, MA1, MA2, and MA8) to the 256K SIMMs on the Micro Innovations
  4  1MB/2MB memory board.
  5
  6
  7  |GAL22V10X 1:CLK,  2:D2,   3:D1,   4:D0,   5:A0,   6:A1,
  8  |          7:A10,  8:A2,   9:D4,   10:D3,  11:A9,  13:MUX,
  9  |          14:A8,  15:MA8, 16:MA2, 17:MA1, 18:MA0, 19:D1L,
 10  |          20:D0L, 21:D4L, 22:D3L, 23:D2L
 11  |
 12  |          D0L = CLK \\ D0
 13  |          D1L = CLK \\ D1
 14  |          D2L = CLK \\ D2
 15  |          D3L = CLK \\ D3
 16  |          D4L = CLK \\ D4
 17  |          MA0 = (A0 & MUX') + (A8 & MUX)
 18  |          MA1 = (A1 & MUX') + (A9 & MUX)
 19  |          MA2 = (A2 & MUX') + (A10 & MUX)
 20  |          MA8 = (D0L & MUX') + (D1L & MUX)
 21  |
 22  |          Signature: "2MU1rev0"
```

RESOLVED EXPRESSIONS (Reduction 2)

Signal name	Row	Terms
D0L	35	D0
D1L	50	D1
D2L	2	D2
D3L	11	D3
D4L	22	D4
MA0	67	A0 MUX'
	68	MUX A8
MA1	84	A1 MUX'
	85	A9 MUX
MA2	99	A10 MUX
	100	A2 MUX'
MA8	112	MUX' D0L
	113	MUX D1L

♀SIGNAL ASSIGNMENT

Pin	Signal name	Column	Rows Beg	Rows Avail	Rows Used	Activity	
1.	CLK	0	-	-	-	High	(Clock)
2.	D2	4	-	-	-	High	

3.	D1	8	-	-	-	High	
4.	D0	12	-	-	-	High	
5.	A0	16	-	-	-	High	
6.	A1	20	-	-	-	High	
7.	A10	24	-	-	-	High	
8.	A2	28	-	-	-	High	
9.	D4	32	-	-	-	High	
10.	D3	36	-	-	-	High	
11.	A9	40	-	-	-	High	
13.	MUX	42	-	-	-	High	
14.	A8	38	122	9	0	High	(Registered)
15.	MA8	34	111	11	2	High	(Three-state)
16.	MA2	30	98	13	2	High	(Three-state)
17.	MA1	26	83	15	2	High	(Three-state)
18.	MA0	22	66	17	2	High	(Three-state)
19.	D1L	19	49	17	1	High	(Registered)
20.	D0L	15	34	15	1	High	(Registered)
21.	D4L	11	21	13	1	High	(Registered)
22.	D3L	7	10	11	1	High	(Registered)
23.	D2L	3	1	9	1	High	(Registered)
25.	-	-	0	1	0		
26.	-	-	131	1	0		
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				132	13	(10%)	

I200 No fatal errors found in source code.
I201 No warnings.

♀OrCAD PLD
Type: PAL22V10
*
QP24* QF5828* QV1024*
F0*
L0044 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0088 11 11 01 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0440 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0484 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 01 11 11 *
L0924 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0968 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 01 11 11 11 11 11 *
L1496 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L1540 11 11 11 11 11 11 01 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L2156 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L2200 11 11 11 11 01 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L2904 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L2948 11 11 11 11 11 11 11 11 01 11 11 11 11 11 11 11 11 11 11 11 11 10 *
L2992 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 01 11 01 *
L3652 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L3696 11 11 11 11 11 11 11 11 11 11 01 11 11 11 11 11 11 11 11 11 11 10 *
L3740 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 01 01 *
L4312 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L4356 11 11 11 11 11 11 11 11 11 11 11 11 01 11 11 11 11 11 11 11 11 01 *
L4400 11 11 11 11 11 11 11 11 11 11 11 11 11 11 01 11 11 11 11 11 11 10 *
L4884 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L4928 11 11 11 11 11 11 11 10 11 11 11 11 11 11 11 11 11 11 11 11 11 10 *
L4972 11 11 11 11 11 11 11 11 11 10 11 11 11 11 11 11 11 11 11 11 11 01 *
L5808 10 10 10 10 10 11 11 11 11 11 *
C76E8*

I202 4/29/92 5:04 pm (Wednesday)
I203 Memory utilization 1562/22426 (7%)

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I204  Elapsed time 2 seconds
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